REMARKS

Prior to entry of this amendment, claims 1-22 are pending. By this amendment, claims 2 and 21-22 are canceled, claims 1, 3, 8, 9, 14 and 15 are amended, and new claims 23-28 are added. The subject matter of the amendments to claims 1, 3, 8, 9, 14 and 15 and new claims 23-28 is fully supported in the specification as filed, and thus, no new matter is added.

Favorable reconsideration of this application is respectfully requested in view of the following remarks.

Claims 1, 3-20 and 23-28 are presented for prosecution on the merits.

In the Office Action mailed July 12, 2004, claims 3-8, 14, and 15 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 3, 8, 14 and 15 have been amended responsive to this rejection. If any additional amendment is necessary to overcome this rejection, the Examiner is requested to contact the Applicant's undersigned representative.

Claims 1, 3, 4, 8, 9, 14 and 15 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No.: 6,034,563 to Mashiko (hereinafter, "Mashiko"), claims 2, 5-7, 10-13 and 16-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashiko. It is noted that claims 1, 3, 8, 9, 14 and 15 have been amended and claims 2 and 21-22 have been canceled. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

In rejecting claims 1 and 8 and claims dependent thereon, the Office Action asserts that the load circuit of these claims is taught by circuit 11 of Fig. 1 of Mashiko.

Claims 1 and 8 recite, in part:

> a load circuit...wherein: a second power supply terminal of said load circuit is connected to a **real** low-potential power supply line; [emphasis added]

As illustrated in Fig. 1 of Mashiko, the logic circuit 11 has one terminal connected to the pseudo high-potential power supply line, and a second terminal connected to the **pseudo** low-potential power supply line.

Therefore, Mashiko fails to disclose a second power supply terminal of said load circuit is connected to a real low-potential power supply line, as recited in claims 1 and 8. Consequently, logic circuit 11 cannot be the load circuit recited in claims 1 and 8.

Further, in Fig. 1 of Mashiko, a p type (high-threshold P-channel type) MOS transistor Q1 is connected to logic circuit 11 through the pseudo high-potential power supply line VDD_v, and an n type (high-threshold N-channel type) MOS transistor Q2 is connected to the logic circuit 11 through pseudo low-potential power supply line GND_v In Fig. 12(A) of Mashiko, an n type MOS transistor Q3 is connected to a logic circuit 53 through VDD_v and an n type MOS transistor Q4 is connected to the logic circuit 53 through GND_v In addition, Mashiko discloses at col. 13, lines 8-10 that the n type MOS transistor Q3 may be removed and the logic circuit 53 is connected directly to VDD (real high-potential power supply line) as shown in FIG. 12(A).

In claims 1 and 8, there is no high-threshold N-channel type MIS field effect transistor provided between the real low-potential power supply line and the pseudo low-potential power supply line as in Mashiko.

Furthermore, claims 1 and 8 recite, in part:

> a back gate of said low-threshold P-channel type MIS field effect transistor is connected to said pseudo high-potential power supply line

Mashiko neither discloses nor suggests a back gate of a low-threshold P-channel type MIS field effect transistor that is connected to the pseudo high-potential power supply line as recited in claims 1 and 8.

Claim 8 further recites, in part:

> a high-threshold N-channel type MIS field effect transistor connected between a real high-potential power supply line and a pseudo high-potential power supply line, said high-threshold N-channel type MIS field effect transistor being controlled by receiving a slowly rising control signal to a gate thereof; and

As recited in claim 8, the high-threshold N-channel type MIS field effect transistor is controlled by receiving a slowly rising control signal at a gate thereof.

However, Mashiko neither discloses nor suggests that the "high-threshold N-channel type MIS field effect transistor being controlled by receiving a slowly rising control signal to a gate thereof."

Applicants respectfully submit that for at least the above reasons, claims 1 and 8 and claims dependent thereon are patentably distinct over Mashiko and in condition for allowance.

Claim 9 recites, in part:

> second power supply terminal of said load circuit is connected to a second real power supply line;

In rejecting claim 9, the Office Action asserts that the load circuit of claim 9 reads on circuit 11 of Fig. 1 of Mashiko. As illustrated in Fig. 1 of Mashiko, the logic circuit 11 has two terminals: one terminal connected to the **pseudo** high-potential power supply line, and a second terminal connected to the **pseudo** low-potential power supply line.

However, Mashiko does not show a connection to a second real low-potential power supply line.

Therefore, Mashiko fails to disclose a "second power supply terminal of said load circuit is connected to a second real low-potential power supply line," as recited in claim 9.

Claim 9 also recites, in part:

> a waveshaping circuit which receives the output signal of said level conversion circuit, and performs waveshaping so that the output signal of said level conversion circuit rises slowly, wherein:
> ...an output signal of said waveshaping circuit is supplied to the gate of said high-threshold MIS field effect transistor of said first conductivity type.

As recited in claim 9, the waveshaping circuit receives the output signal of the level conversion circuit and performs waveshaping such that the signal rises slowly. An output signal of the waveshaping circuit is supplied to a gate of the high-threshold MIS field effect transistor.

Mashiko neither discloses nor suggests the waveshaping circuit receives the output signal of the level conversion circuit and performs waveshaping such that the signal rises slowly, and an output signal of the waveshaping circuit is supplied to a gate of the high-threshold MIS field effect transistor, as recited in claim 9.

Therefore, Applicants respectfully submit that claim 9 is patentably distinct over Mashiko and in condition for allowance.

As claims 3-7 depend from claim 1 and claims 10-20 depend from claim 9, claims 3-7 and 10-20 are allowable for at least the reasons claims 1 and 9 are allowable.

New claims 23-28 depend from one of claims 1, 8 and 9 and as such, Applicants respectfully submit that each of claims 23-28 is allowable for at least the reasons claims 1, 8 and 9 are allowable.

Conclusion

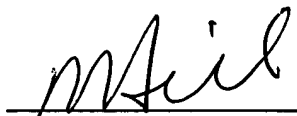
For all of the above reasons, it is respectfully submitted that claims 1, 3-20 and 23-28 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 **referencing client matter number 100021-00133.**

Respectfully submitted,

Arent Fox, PLLC



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